Parallel Interleaver Design for High Throughput Configurable Turbo Decoder

Guohui Wang, Aida Vosoughi, and Joseph R. Cavallaro
Department of Electrical and Computer Engineering, Rice University

BACKGROUND

- Turbo decoder is essential for 3G/4G wireless communication systems [1];
- Parallel architecture is required for high throughput turbo decoder;
- $P$ parallel soft-input soft-output (SISO) decoders are used to decode a $K$-bit codeword.

CHALLENGES

The information memory is partitioned into $M$ banks. If two or more SISO decoders attempt to access a same memory bank $m$, a memory conflict occurs. Memory conflict can significantly reduce decoding throughput.

PARALLEL IAG ARCHITECTURE

A unified interleaver address generation (IAG) architecture supporting both interleaving and deinterleaving algorithms [3].

Memory conflict problem is difficult to solve due to:
1. High throughput requirement;
2. High parallelism degrees (4, 8, 16, 32 and up);
3. Diverse SISO decoder design (SMAP, XMAP, ...);
4. Multi-standard support (HSPA+, LTE and so on);
5. High hardware complexity to implement interleaving algorithms.

NEW SCHEDULING SCHEME [3]

Original scheduling:

Proposed new scheduling:

Main benefits:
1. Eliminate memory reading collisions;
2. Reduce hardware complexity;
3. More balanced workload between half-iterations.

DBCF BUFFER STRUCTURE [2]

We proposed double-buffer contention-free (DBCF) buffer structure to solve the memory writing conflict problem in parallel turbo decoder [2].

IMPLEMENTATION RESULTS

The table shows synthesis results for the proposed parallel interleaver under a TSMC 65nm technology.

<table>
<thead>
<tr>
<th>Parallelism $P$</th>
<th>Frequency $f_{\text{max}}$</th>
<th>Area $[\text{mm}^2]$</th>
<th>Throughput $\text{Mbit/s}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>700 MHz</td>
<td>0.040</td>
<td>136 Mbit/s</td>
</tr>
<tr>
<td>8</td>
<td>700 MHz</td>
<td>0.076</td>
<td>230 Mbit/s</td>
</tr>
<tr>
<td>16</td>
<td>700 MHz</td>
<td>0.146</td>
<td>455 Mbit/s</td>
</tr>
<tr>
<td>32</td>
<td>700 MHz</td>
<td>0.285</td>
<td>899 Mbit/s</td>
</tr>
</tbody>
</table>

To conclude, with new scheduling scheme, the unified parallel IAG and DBCF buffer structure, the proposed parallel interleaver:
- solve memory conflict problem for highly parallel turbo decoder;
- support high throughput turbo decoding with low hardware complexity;
- support multiple standards, such as HSPA+, LTE and etc.

REFERENCES